

# Ultra-Energy-Efficient Polar Decoder ASIC IP Core

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## I. HIGHLIGHTS

- **0.68 pJ/b energy efficiency** with 128 Gb/s throughput at 150 MHz clock frequency
- Optimized for minimum area and low power
- Full timing-clean implementation in EPIC<sup>1</sup> project at 16nm TSMC FinFET technology
  - 0.22 mm<sup>2</sup> area, 86.76 mW power dissipation
- 6.21 dB coding gain at 10<sup>-12</sup> Bit Error Rate (BER)
  - Much higher coding gain options are available with low power outer codes.
- 80 ns latency (12 pipeline stages)
- Potential use-cases for the IP core include fiber-optic, wireline and intra-chip communications
- White box licensing available

## II. ARCHITECTURE DETAILS

- Block length (*N*) of 1024 bits and the payload (*K*) of 854 bits with 20% coding overhead
- Successive Cancellation (SC) decoding algorithm
  - Unrolled pipelined architecture
  - Pipeline optimization, register reduction and retiming
  - Optimized multi-bit parallel decision shortcuts
  - Adaptive quantization of (LLR) metrics
- Fully verified end-to-end FPGA implementation with 9 sigma AWGN simulator (demonstrated at EUCNC-2019 and MWC-2020)
- Testbench, test-vectors, indicator vector of the frozen/free bits and support files are available on demand
- Customizable to other *N* and *K* on demand

## III. IP BLOCK DESCRIPTION

The input-output block diagram of the decoder IP core is shown in Fig. 1.

- All synchronous logic operations are triggered by the rising edge of system clock at the *clk* pin.
- The *clk\_en* input marks the beginning of valid input data.
- A synchronous active-high *reset* signal resets all registers within 5 clock cycles.
- The *data\_in* is a 5120-bit wide input port for receiving 1024 input log-likelihood ratio (LLR) metrics, with 5-bit precision per LLR

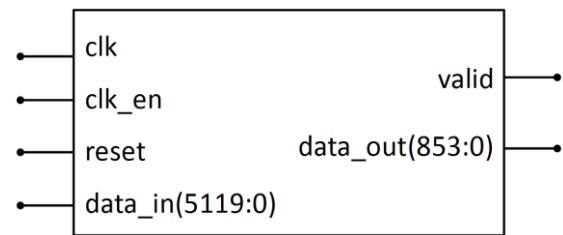


Figure 1: Block diagram of the IP core

- The *data\_out* is a 854-bit output port for outputting the decoded data bits.
- The *valid* output signal marks valid signals at the *data\_out* port.

FPGA simulation results for the BER and Frame Error Rate (FER) performance of the IP core are shown in Fig. 2.

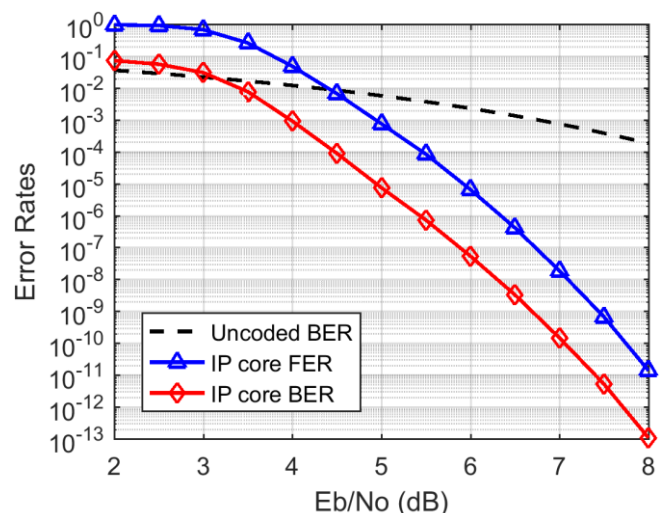


Figure 2: Error correction performance of the IP core

The IP core has been implemented (virtual tape-out) within the EPIC project using 16nm technology and the following results were obtained.

Parameter	Result
Throughput	128.1 Gb/s
Area	0.217 mm <sup>2</sup>
Power	86.76 mW
Energy-per-bit	0.68 pJ/bit
Latency	80 ns

<sup>1</sup>EPIC is a project of the European Union’s Horizon 2020 Research and Innovation Programme under Grant Agreement no. 760150.



POLARAN LTD ([www.polaran.com](http://www.polaran.com)) offers a full range of IP cores for implementation of polar codes on FPGA or ASIC platforms. For further information, please contact Polaran at [info@polaran.com](mailto:info@polaran.com) or at +90-312-2650224.