One Terabit/s Polar Decoder ASIC IP Core

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I. HIGHLIGTHS

- **1 Tb/s throughput** at 1.2 GHz clock frequency
- Optimized for minimum area and low power
- Full timing-clean implementation in EPIC[1] project at 16nm TSMC FinFET technology
  - 0.8 mm^2, 1.14 pJ/b energy consumption
- 6.21 dB coding gain at 10^{-12} Bit Error Rate (BER)
  - Much higher coding gain options are available with low power outer codes.
- 49 ns latency (59 pipeline stages)
- Potential use-cases for the IP core include fiber-optic, wireline and intra-chip communications
- White box licensing available

II. ARCHITECTURE DETAILS

- Block length (*N*) of 1024 bits and the payload (*K*) of 854 bits with 20% coding overhead
- Successive Cancellation (SC) decoding algorithm
  - Unrolled pipelined architecture
  - Pipeline optimization, register reduction and retiming
  - Optimized multi-bit parallel decision shortcuts
  - Adaptive quantization of (LLR) metrics
- Fully verified end-to-end FPGA implementation with 9 sigma AWGN simulator (demonstrated at EUCNC-2019 and MWC-2020)
- Testbench, test-vectors, indicator vector of the frozen/free bits and support files are available on demand
- Customizable to other *N* and *K* on demand

III. IP BLOCK DESCRIPTION

The input-output block diagram of the decoder IP core is shown in Fig. 1.

- All synchronous logic operations are triggered by the rising edge of system clock at the *clk* pin.
- The *clk_en* input marks the beginning of valid input data.
- A synchronous active-high *reset* signal resets all registers within 5 clock cycles.
- The *data_in* is a 5120-bit wide input port for receiving 1024 input log-likelihood ratio (LLR) metrics, with 5-bit precision per LLR

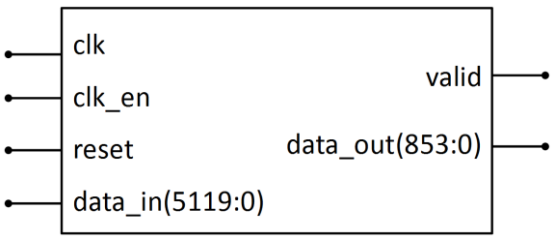

Figure 1: Block diagram of the IP core

- The *data_out* is a 854-bit output port for outputting the decoded data bits.
- The *valid* output signal marks valid signals at the *data_out* port.

FPGA simulation results for the BER and Frame Error Rate (FER) performance of the IP core are shown is shown in Fig. 2.

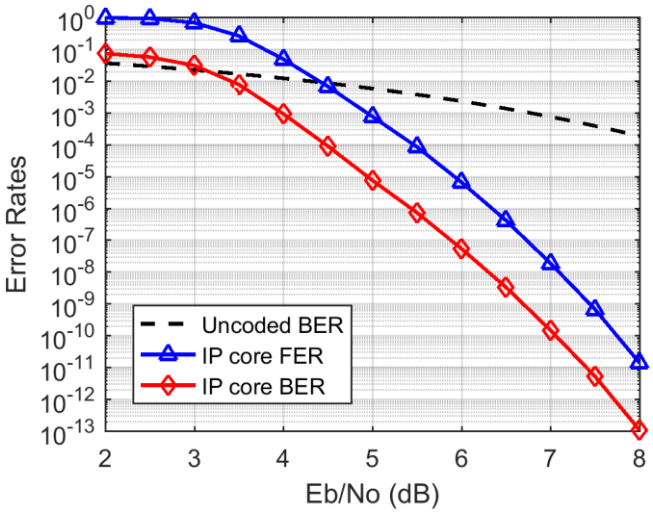

Figure 2: Error correction performance of the IP core

The IP core has been implemented (virtual tape-out) within the EPIC project using 16nm technology and the following results were obtained.

Parameter	Result
Throughput	1025 Gb/s
Area	0.791 mm^2
Power	1167 mW
Energy-per-bit	1.14 pJ/bit
Latency	49 ns

[1]EPIC is a project of the European Union's Horizon 2020 Research and Innovation Programme under Grant Agreement no. 760150.