Polar Decoder (PD-100G)

Features

- Supports 7-Series Xilinx FPGAs (Artix-7, Kintex-7, Virtex-7, Virtex-7 Ultrascale+)
- Satisfies Cloud Radio Access Network (C-RAN) fronthaul requirements in terms of high data throughput, low latency and low energy consumption
- Compatible with Polar codes
- Implements unrolled and pipelined decoding architecture
- Adjustable I/O port size with respect to code block length (N), code rate (R) and payload (K)
- Supports

$$R=\begin{cases}\left(\frac{1}{2},\frac{3}{4},\frac{4}{5},\frac{5}{6},\frac{15}{16}\right) & for\ N=1024\\ \left(\frac{5}{6},\frac{15}{16}\right) & for\ \ N=2048\\ \left(\frac{5}{6}\right) & for\ \ N=8192\end{cases}$$

- Supports 100 Gb/s data speed, and more than 7.5dB coding gain
- Compatible with Xilinx Vivado versions greater than 2016.1

General Description

The PD-100G is designed for C-RAN fronthaul to decode In-phase and Quadrature components of the signal transmitted from Remote Radio Heads (RRH) to Baseband Unit (BBU) Pool through optical links. The decoder satisfies the low latency and high throughput requirements of the optical link between RRH and BBU. The decoder can exceed 100 Gb/s for the provided design configurations.

The decoder is compatible with the IP core products of POLARAN: Polar Combinational Encoder Family

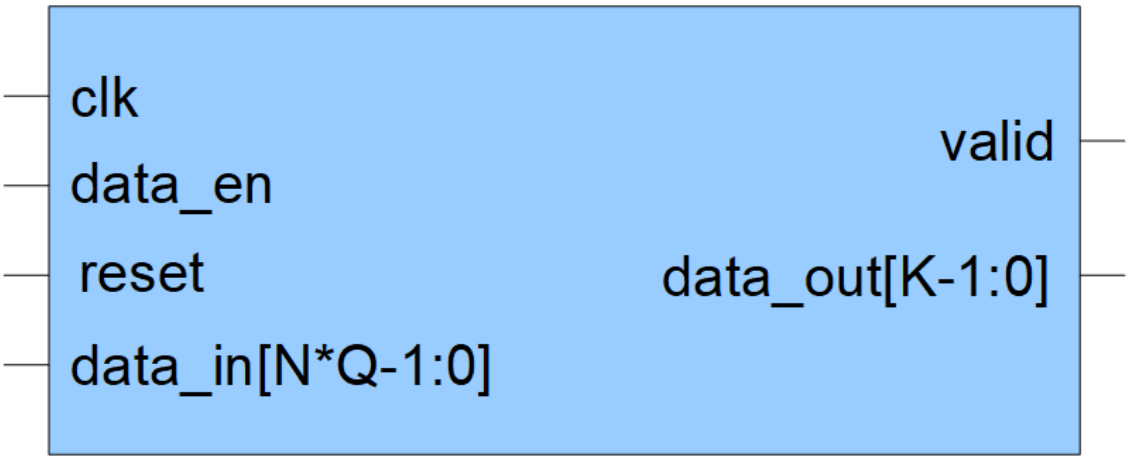

Figure 1: Block Diagram of PD-100G

Input/Output Ports

The descriptions of I/O ports of the PD-100G are stated in Table 1.

Table 1: I/O Ports

Pin	Sense	Port Width (bits)	Description
CLK	Input	1	***Clock.*** All synchronous logic operations are triggered by rising edge of CLK.
DATA_IN	Input	N	***Input Data.*** Encoded data (data bits + parity bits) are given to the decoder through this port. The port width of the encoded data is N.
DATA_EN	Input	1	***Data Enable.*** Marks the valid input data.
DATA_OUT	Output	K	***Output Data.*** Consists of information bits.
VALID	Output	1	***Valid Output Data.*** Marks the valid output data.
PREC	Constant	Q	***Precision.*** Encoded data will be represented with Q bits.

Further explanations about I/O ports are shown below.

Clock (CLK)

All synchronous logic operations of the system are triggered by rising edge of the Clock (CLK).

Data Enable (DATA_EN)

Input data must be applied when data enable is high, otherwise it is discarded.

Input Data (DATA_IN)

Decoder accepts data from this pin. Input data consists of the channel output. At each clock cycle, data width of input data can be applied to the decoder.

Output Data (DATA_OUT)

The decoded data is written on the DATA_OUT port in fully parallel manner. The data width of that port is called “K”. The output data consists of only information bits.

Valid (VALID)

When there is an output data at the DATA_OUT port this signal becomes ‘1’ to signal that system has an output.

Precision (PREC)

Shows how many bits are used to represent encoded data.

Functional Description of Polar Majority Logic Decoder

The behavioral simulation of PD-100G is shown in Figures 2, 3 and 4.

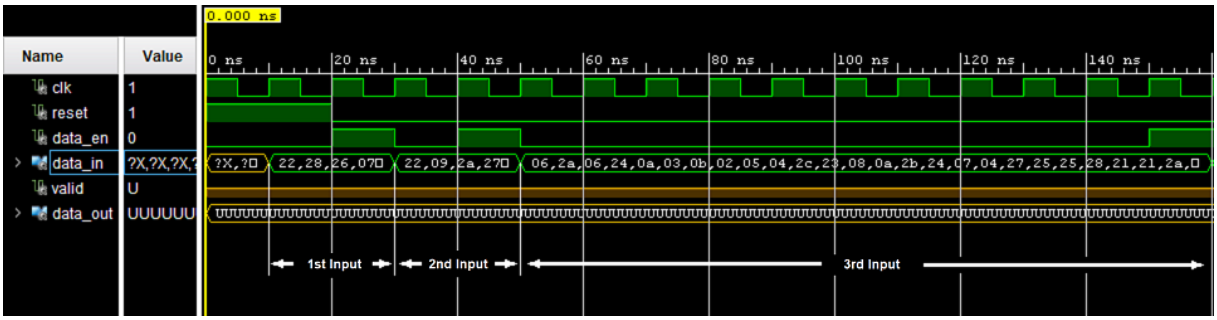

Figure 2: Behavioral Simulation of PD-100G Input Logic (N=1024, R=15/16)

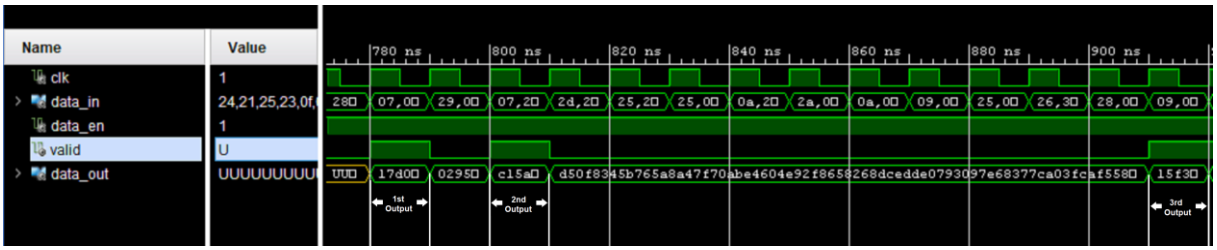

Figure 3: Behavioral Simulation of PD-100G Output Logic (N=1024, R=15/16)

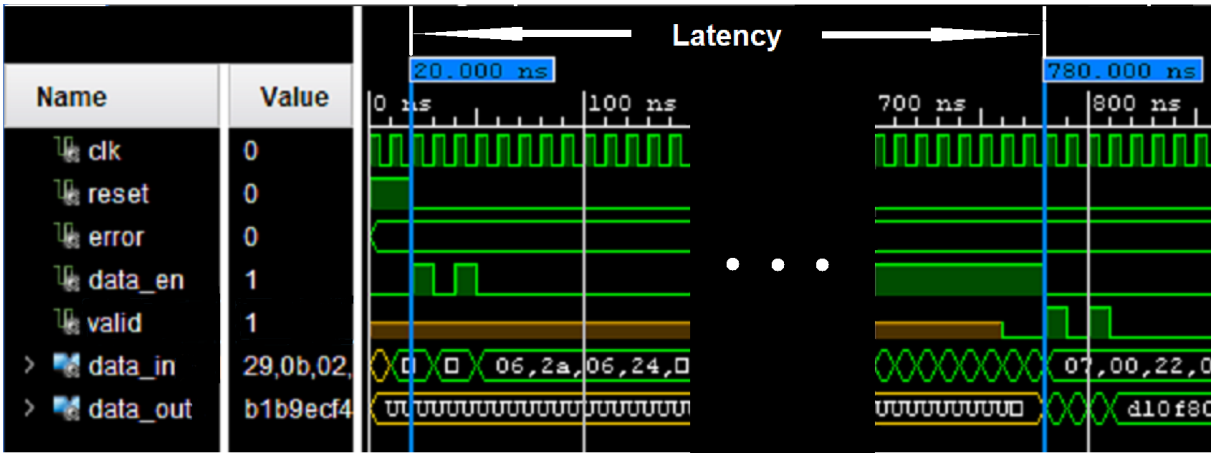

Figure 4: The Behavioral Simulation of PD-100G Latency (N=1024, R=15/16)

PD-100G is a fully parallel pipelined decoder. It can accept input data from “data_in” port at each rising edge of clock, when the “data_en” port is high. When the “data_en” input is low, decoder doesn’t accept input data from “data_in” port. These data are discarded. After decoding process is finished, decoder assigns high to “valid” port and decoded bits are sent through “data_out” port. Since this algorithm is based on Polar codes, latency of decoder gets bigger when block length (N) increases. Also, number of pipeline stages increase when block length (N) increases.

Detailed Information of PD-100G

PD-100G is implemented on either Kintex-7 or Virtex-7 Ultrascale+ Xilinx FPGA. Vivado throughput and resource usage results are shown in Table 2 and Table 3 respectively. Performance results of the decoders are given in Figure 5.

Table 2: PD-100G Throughput Results

FPGA Type	Block Length	Coding Rate	Frequency (MHz)	TP (Gb/s)
Kintex-7 (xc7k325t)	1024	1/2	120	61.44
	1024	3/4	120	92.16
	1024	4/5	120	98.30
	1024	5/6	120	102.48
	1024	15/16	120	115.20
Virtex-7 Ultrascale+ (xcvu9p-flgb2104)	2048	5/6	60	102.48
	2048	15/16	60	115.20
	8192	5/6	25	170.68

Table 3: PD-100G Resource Usage Result

FPGA Type	Quantization Bits	Block Length	Coding Rate	Resource Usage							
				LUT		FF		BRAM		URAM	
				Num.	%	Num.	%	Num.	%	Num.	%
Kintex-7 (xc7k325t)	6	1024	1/2	103712	50.99	58345	14.34	172	38.54		
	6	1024	3/4	90211	44.35	53381	13.12	172	38.54		
	6	1024	4/5	102937	50.61	61429	15.10	172	38.54		
	6	1024	5/6	95858	47.04	56761	13.93	172	38.54	-	-
	6	1024	15/16	61067	29.96	37937	9.31	129	28.99	-	-
Virtex-7 Ultrascale+ (xcvu9p-flgb2104-2-i)	6	2048	5/6	213214	18.03	115449	4.88	471	21.81	-	-
	6	2048	15/16	165571	14.00	86355	3.65	279	12.92	-	-
	2	8192	5/6	297697	25.18	222610	9.41	770	35.63	-	
	4	8192	5/6	642761	54.37	393098	16.63	855	39.58	684	71.25

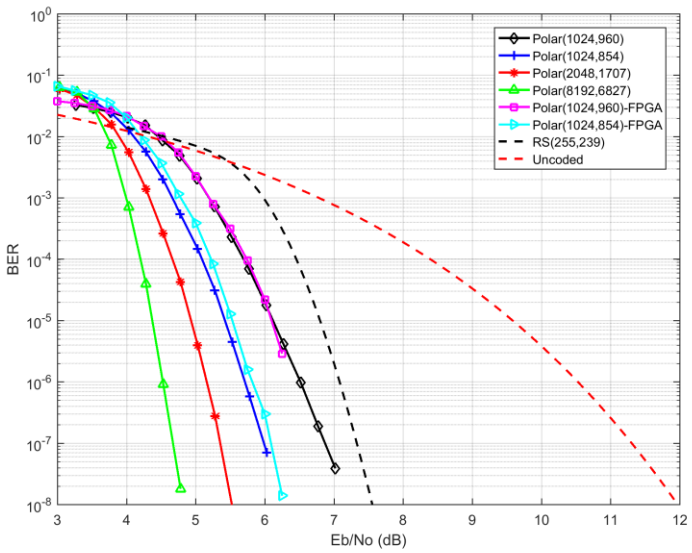

Figure 5: BER performances of the PD-100G family

Document Changelog

Version	Publish Date	Changed Content/Page	Reason
1.0	30.01.2018	Whole report	First version of the report was written.
1.1	24.07.2018	New designs are added, resource usage is updated.	New data.