Main Features of Polar-SC-200G IP Core

- Polar Successive Cancellation 200 Gb/s (Polar-SC-200G) IP Core supports **200 Gb/s** throughput at 235 MHz clock frequency.
- Polar-SC-200G supports code block length (*N*) of 1024 and payload (*K*) of 854 bits with 20% coding overhead. It is customizable to other *N* and *K* on demand.
- Polar-SC-200G employs fully-parallel and unrolled hardware architecture with dedicated processing elements. It exploits pipeline depth optimization, register balancing/retiming and adaptive quantization of LLR metrics.
- The net coding gain of the selected (*N=1024, K=854*) polar code is 6.2 dB at 10^{-12} BER.
- Polar-SC-200G has been tested on Xilinx VCU128 Evaluation Kit with 16nm Virtex Ultrascale+ (xcvu37p-fsch2892-2L-e-es1) FPGA.

Input and Output Ports of Polar-SC-200G IP Core

The block diagram of Polar-SC-200G IP Core is shown in Figure 1.

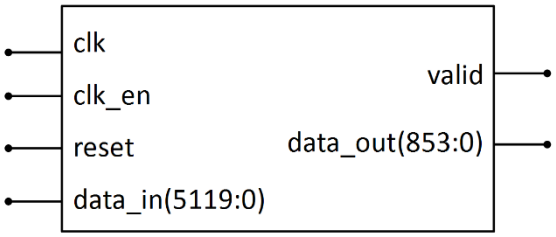

Figure 1: Block diagram of Polar-SC-200G IP Core

- All synchronous logic operations are triggered by the rising edge of system clock at the **clk** pin.
- The **clk_en** input marks the beginning of valid input data.
- A synchronous active-high **reset** signal resets all registers within 5 clock cycles.
- The **data_in** is a 5120-bit wide input port for receiving 1024 input log-likelihood ratio (LLR) metrics, with 5-bit precision per LLR
- The **data_out** is a 854-bit output port for outputting the decoded data bits.
- The **valid** output signal marks valid signals at the data_out port.

Polar Code Specification

Polar-SC-200G IP Core utilizes a polar code with *N*=1024 block length and *K*=854 payload. The polar code has 1024-854=170 frozen (redundancy) coordinates listed below. Note that the frozen coordinates are given in the bit-reversed order.

[1,2,3,4,5,6,7,9,10,11,13,17,18,19,21,25,33,34,35,37,41,45,49,53,57,65,66,67,69,73,77,81,83,85,89,97,99,101,105,113,129,130,131,133,137,141,145,147,149,153,161,163,165,169,177,193,194,195,197,201,209,225,241,257,258,259,261,265,267,269,273,275,277,281,289,290,291,293,297,305,321,322,323,325,329,337,353,361,369,385,386,387,389,393,401,417,425,433,449,453,457,465,481,513,514,515,517,521,523,525,529,530,531,533,537,545,546,547,549,553,561,577,578,579,581,585,593,609,617,625,641,642,643,645,649,657,665,673,681,689,705,709,713,721,737,769,770,771,773,777,785,793,801,805,809,817,833,837,841,849,865,897,899,901,905,913,929,961,977, 993]

Bits of frozen coordinates can be chosen arbitrarily but all are assigned to zero to maximize the advantage of shortcuts encountered in SC decoding algorithm. The remaining 854 free coordinates carry data bits. The given polar code design is constructed using Density Evolution algorithm optimized at 6.5 dB SNR.

Polar-SC 200G IP Core FPGA Architecture

This section describes the unrolled SC architecture, adaptive quantization and register balancing/retiming methods

Unrolled SC Architecture: Unrolled SC decoder architecture restricts logic reuse but promotes a dedicated hardware for each calculation. This allows codeword pipelining and maximizes the throughput at the cost of memory for storing codewords and corresponding hard decisions. The recursive structure of SC algorithm enables limited number of instructions. There are only 7 unique instructions to define every calculation in SC decoder. Any polar SC decoder can be generated with a specific order of the given instructions. The unrolled architecture of Polar-SC200G consists of heavily pipelined stages. When we decrease pipeline stages, depth of this memory also decreases.

Advanced quantization: Advanced quantization is an optimization method to reduce hardware complexity by decreasing LLR bit precision of internal data paths in the SC decoder. Instead of storing and processing LLRs with a constant resolution, a variable number of bits are used for each polar code segment. During SC decoding of polar codes, polarization increases as we go deep into decoding stages. As polarization increases, so does the reliability of the bits, hence the resolution of LLRs can be decreased without significant performance difference An advanced quantization scheme used in Polar-SC-200G is shown in Figure 2. The number of quantization bits are written on the lines between polar code segments. With the advanced quantization, the memory complexity is reduced by 15.1% while having 4.25-bit average LLR bit precision.

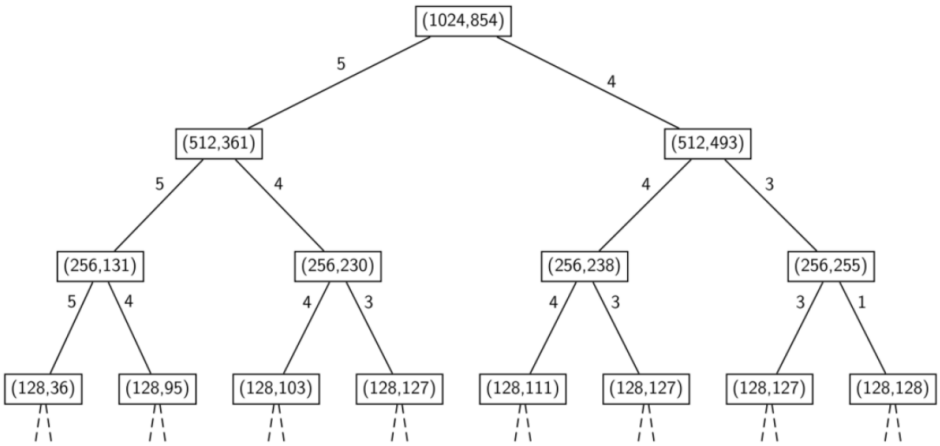

Figure 2: Advanced quantization scheme used in Polar-SC-200G IP Core

Register balancing/retiming: Pipeline stages are important to manage the critical path and, thus, achieve the target clock frequency. Hence for an efficient hardware implementation, reducing number of pipeline stages is a critical optimization step. For this purpose, we merge a set of consecutive short calculations of the SC decoder based on the combinational delay from timing simulations. Register reduction is challenging for SC decoding algorithm due to its sequential essence. We overcome this problem by estimating the delay of each sequential computation. Polar-SC-200G has remarkably reduced latency and memory consumption due to register balancing/retiming.

FPGA Test Platform

Polar-SC-200G is verified under AWGN channel, which is also implemented on FPGA. The FPGA test platform shown in Figure 3 also includes a compatible systematic polar encoder, BPSK mapper and SISO LLR de-mapper modules. Initially, an LFSR based Random Number Generator (RNG) generates 854-bit pseudo-random information bits. These bits are encoded by Polar Encoder to generate a valid polar codeword with 1024 parity and information bits. Then, BPSK Mapper takes 1024-bit input from the Polar Encoder module and maps the encoded bits to the +1 and -1 symbols where each symbol has 16-bit precision. The AWGN Channel module combines the symbols with channel noise, which is generated from Gaussian Number Generator (GNG) module. SISO LLR De-mapper transforms the channel output to LLRs, each having 5-bit precision including 3-bit fractional part. After that, Polar-SC-200G IP Core receives LLRs and calculates an estimate of the transmitted information sequence. Finally, BER/FER Calculator module compares the estimated information sequence with the original sequence and calculates the BER and FER of the target polar code.

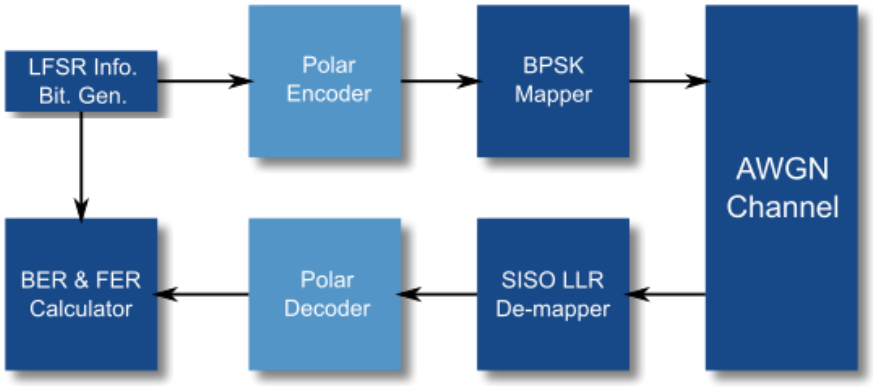

Figure 3: Block diagram of the FPGA test platform used for the verification of Polar-SC-200G IP Core

Communication Performance of Polar-SC-200G IP Core

FPGA simulations have been carried out for a set of Eb/No values from 2 to 8.5 dB with 0.5 dB step size. The FPGA simulation results Figure 4 show that a coding gain of 6.21 dB is attained at 10^{-12} BER relative to uncoded transmission.

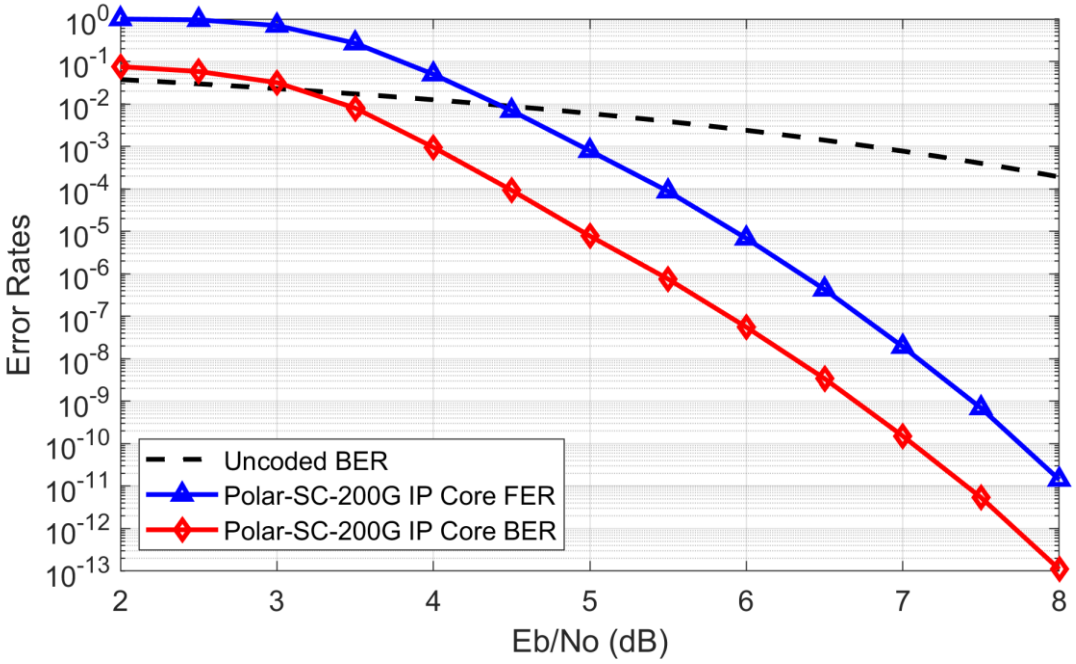

Figure 4: BER/FER performance of Polar-SC-200G IP Core

FPGA Implementation Results

The implementation results of polar encoder, Polar-SC-100G and Polar-SC-200G IP Cores on Xilinx Virtex Ultrascale+ FPGA is shown in Table 1. Percentages indicate the resources consumed as a fraction of total resources. Polar-SC-200G utilizes more LUT and FF than Polar-

SC-100G, because it has longer pipeline depth and fewer number of slow accessible BRAMs to attain 200 Gb/s throughput. Polar-SC 200G IP core utilizes only 7.4% of the whole FPGA and dissipates 2.4 W power.

Table 1: FPGA implementation results of polar encoder, Polar-SC-100G and Polar-SC-200G IP Cores

	LUT	FF	BRAM	Latency	Clock Freq.	Throughput	Power
Polar Encoder	1,842 (0.14%)	1,825 (0.07%)	-	2 CCs 16 ns	125 MHz	106.75 Gb/s	5 mW
Polar-SC-100G IP Core	53,247 (4.08%)	35,192 (1.35%)	136 (6.75%)	59 CCs 472 ns	125 MHz	106.75 Gb/s	391 mW
Polar-SC-200G IP Core	95,653 (7.34%)	50,700 (1.95%)	72 (3.55%)	158 CCs 672 ns	235 MHz	200.69 Gb/s	2.4 W

FPGA Demo of Polar-SC-200G IP Core

FPGA demo picture of Polar-SC-200G IP Core is shown in Figure 5. Demo type (IP core configuration) and other demo parameters such as number of trials, the Eb/No range, etc. are selected on a PC using a GUI and the corresponding configuration file is uploaded to an FGPA through a JTAG cable. The throughput, BER/FER figures, and latency are displayed on the PC screen in real-time as the simulation takes place on the FPGA.

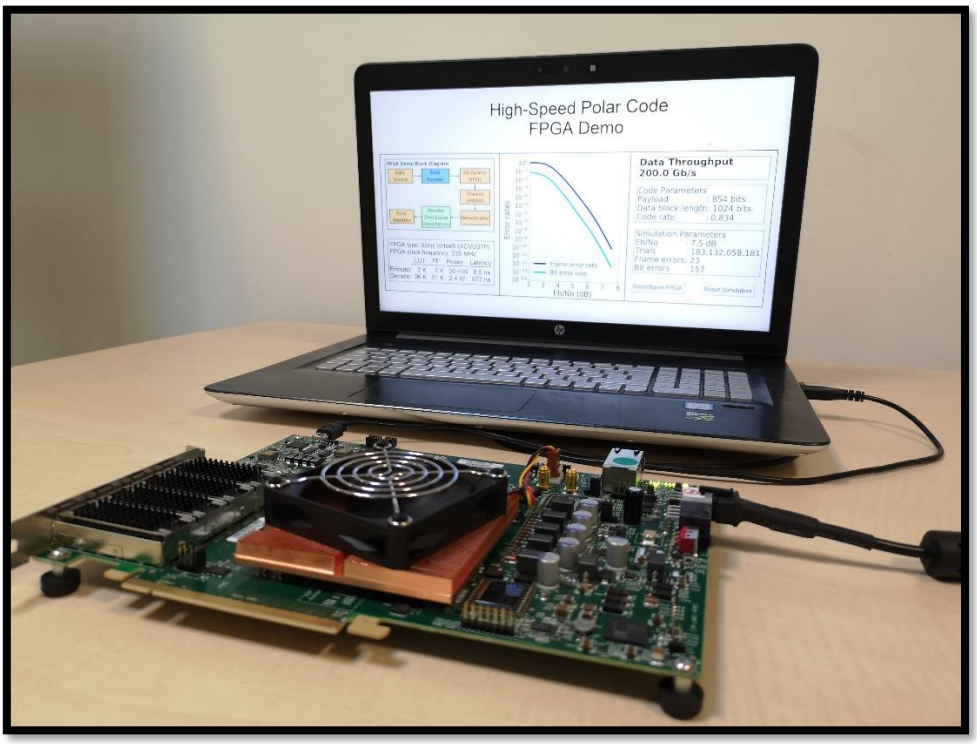

Figure 5: FPGA demo picture of Polar-SC-200G IP Core

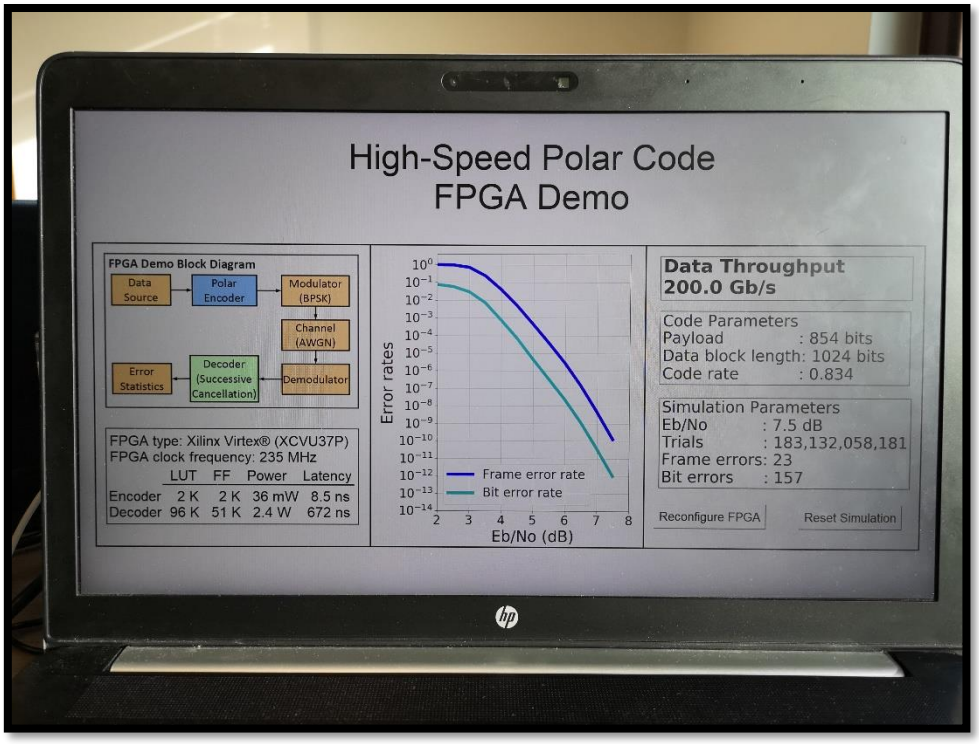

Figure 6: FPGA demo screenshot of Polar-SC-200G IP Core

Document Changelog

Version	Publish Date	Changed Content/Page	Reason
1.0	02.09.2020	All parts	First version was written. IP Core implementation and communication performance results are added.

For more detailed information, please send an email to info@polaran.com.

We may provide the following inputs to our customers:

- Polar code structure and the indicator vector of the frozen/free bits.
- A replica of the HDL polar decoder in software to perform fixed-point simulation and verification.
- Testbench and test-vectors.
- Detailed behavioral documentation of the polar decoder.