White Paper

Polar Codes for Cloud RAN Applications

Polar Codes for Cloud RAN Applications

Polaran LTD.

August, 2018

Table of Contents

List of Figures

List of Tables

1. Executive Summary

The rising demand for network capacity and increasing energy consumption of the fronthaul link has led to centralized Radio Access Network (RAN) architectures, named Cloud-RAN (C-RAN), where the centralized baseband unit (BBU) pools are connected to the remote radio head (RRH) units using fiber links. C-RAN aims to improve the energy efficiency of the fronthaul link and reduce the network management costs.

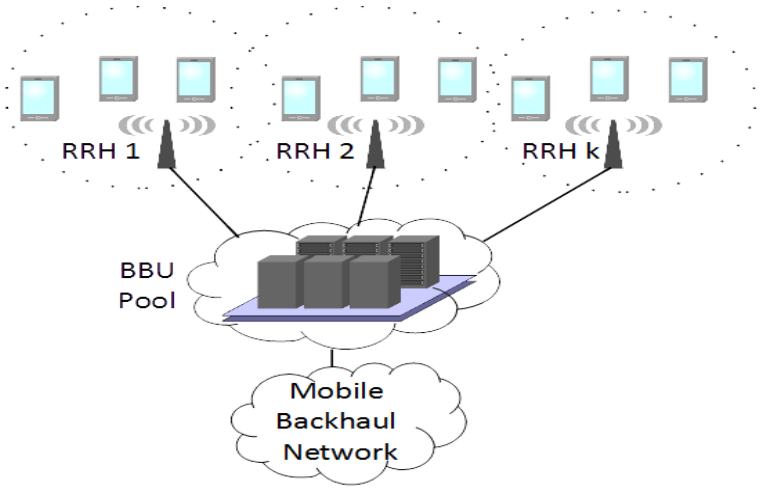

Figure 1: C-RAN Architecture

In order to provide both high throughput and reliable communication between RRH units and the BBU pool we proposed a low-complexity and an energy efficient FEC solution based on polar coding. Polar code encoders and decoders are developed with various configurations to meet the requirements of C-RAN. The performance of the polar encoders and decoders are demonstrated on FPGA with real-time end-to-end tests for benchmarking and measurements. The measurements indicate that the 8192-length polar code decoder reaches 100 Gb/s throughput and 10 dB coding gain.

The polar decoder employs a modified Successive Cancellation (SC) algorithm based on Majority-Logic (MJL) decoding. Although SC is a low-complexity sequential decoding algorithm [1], the data dependencies of the intermediate calculation steps cause throughput and latency bottlenecks. For relaxing the data dependencies and making parallel hard decisions, we proposed a complex but fully-parallel MJL algorithm. The integration of SC and MJL algorithms

established a favorable tradeoff between complexity and throughput, when unrolled and pipelined implementation architecture is utilized. Due to the pipelined architecture the decoder can process a new codeword for every clock cycle and the throughput does not depend on the long latency of the SC decoder. In addition to that the unrolled processing modules perform limited number of operations to restrict the complexity of the decoder.

2. System Requirements

The FEC requirements for the fronthaul link of the C-RAN architecture are [2], [3]:

- **Throughput** ≥ 100 Gb/s
- **Coding Gain** ≥ 10 dB at 10-15 BER
- **Coding Overhead** ≤ 20 %
- **Energy Consumption** ≤ 40 pJ/b
- **Power Dissipation** ≤ 4 W

3. Polar Code Implementations

This section presents the brief introduction and implementation results of the PE-100G and PD-100G members. In subsection 3.1, general properties of the PE-100G and PD-100G; in subsection 3.2, FPGA implementation results of the cores and in subsection 3.3, performance results are presented.

3.1. Introduction of the VHDL IP soft cores

In this section, 3rd generation FEC compatible PE-100G and PD-100G are discussed. PE-100G and PD-100G members are compatible with their counterpart in the other family. IP cores are coded in VHDL and synthesized with Xilinx Vivado version 2018.1. IP cores are designed according to C-RAN algorithm and they provide high throughput with low latency. PD-100G family members are able to pass the required 100 Gb/s net throughput.

In Figure 2, block scheme of the PE-100G is presented. *Data_in* signal is the main input signal of the PE-100G, its length is equal to the number of information bits. *Clk* signal is the synchronous clock signal of the encoder. *Data_en* input signal informs the system that information at the *data_in* port is *valid* and can be used, when the *data_en* is low, the system ignores the information at the *data_in* port. D*ata_out* output signal is the main output signal of the system; it carries out the encoded bits. Length of the *data_out* port is equal to block length. *Valid* out signal carries out the similar task with data_en port. It marks the output at the data_out as valid, if the *valid* signal is low, data at the *data_out* should be ignored.

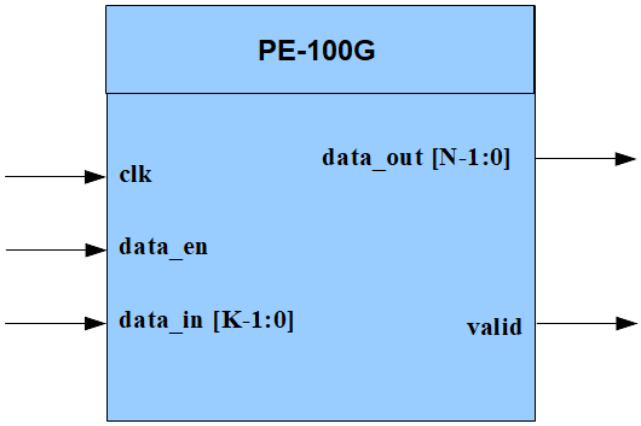

Figure 2: Block scheme of the PE-100G

In Figure 3, block scheme of the IP cores are presented. *Data_in* signal is the main input signal of the system and it carries the information bits. Block length and quantization of this signal are represented with 'N' and 'Q' respectively. Reset input signal is the synchronous reset signal of the system and it resets all of the system to its initial state. *Data_out* output signal is the main output signal of the system; it carries out the decoded bits. Length of this port is represented with 'K' and it depends on the block length (N) and code rate (R) of the system. *Data_en*, *valid* and *clk* signals carry the same properties in PE-100G and PD-100G.

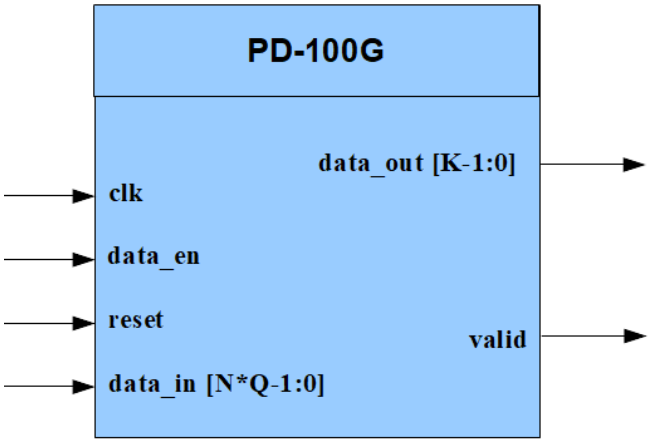

Figure 3: Block scheme of the PD-100G

3.2. Implementation results of the IP soft cores

In this section, implementation results of the developed VHDL IP soft cores are presented. Four different IP cores are discussed: two different block lengths (1024, 2048) and two different code rates (5/6, 15/16) for each block length. Implementations of the IP cores, both PE-100G and PD-100G family, are done on Kintex-7 FPGA.

In Table 1, resource utilization of PE-100G members are given. Polar code encoder is relatively simple design. Therefore, resource usages of the encoders are quite small and can be implemented on relatively cheap FPGAs. Their resource usage for Kintex-7 is under 5% even for the most complex PE-100G family member.

Table 1: Resource utilization results of the PE-100G

FPGA Type	Block Length (N)	Coding Rate (R)	Resource Usage			
			Lut		FF	
			Num.	%	Num.	%
Kintex-7 (xc7k325t)	1024	5/6	2146	1.05	1880	0.46
	1024	15/16	1170	0.57	1986	0.48
	2048	5/6	7480	3.67	3757	0.92
	2048	15/16	3667	1.79	3970	0.97

6 bits quantization is used for PD-100G members because performance of the decoders when the quantization is taken as 6 bits is almost equal to the performance calculated by the infinite precision software simulations. In Table 2, resource utilization of the PD-100G members are given. The design with 2048 block length and 5/6 code rate could not fit into the Kintex-7, so to implement this design bigger FPGA is needed. Other designs are able to fit into the Kintex-7. Memory requirement of the IP soft cores are high; therefore, both Flip-Flop (FF) and Block RAM (BRAM) resources available in the Kintex-7 FPGA are used as memory units. As logic units, Look-Up Table (LUT) resources are used.

Table 2: Resource utilization results of the PD-100G

FPGA Type	Block Length (N)	Coding Rate (R)	Resource Usage					
			LUT		FF		BRAM	
			Num.	%	Num.	%	Num.	%
Kintex-7 (xc7k325t)	1024	5/6	95858	47.04	56761	13.93	172	38.54
	1024	15/16	61067	29.96	37937	9.31	129	28.99
	2048	5/6	213214	104.62	115449	28.32	471	105.84
	2048	15/16	165571	81.24	86355	21.19	279	62.70

3.3.Performance results of the IP soft cores

The polar encoder and decoder modules are embedded in a software and a hardware simulation chain including BPSK modulation and AWGN channel modules. Figure 4 shows the software simulation and FPGA implementation performance of the polar decoders. The implementation loss is negligible when the LLR values are represented with 6 bits. The theoretical performance of polar decoders is shown in Figure 5. With respect to the BEC upper bound, 10 dB coding gain is achieved for only the (65536, 54614) decoder configuration as it reaches 10^{-15} BER before 5 dB Eb/No.

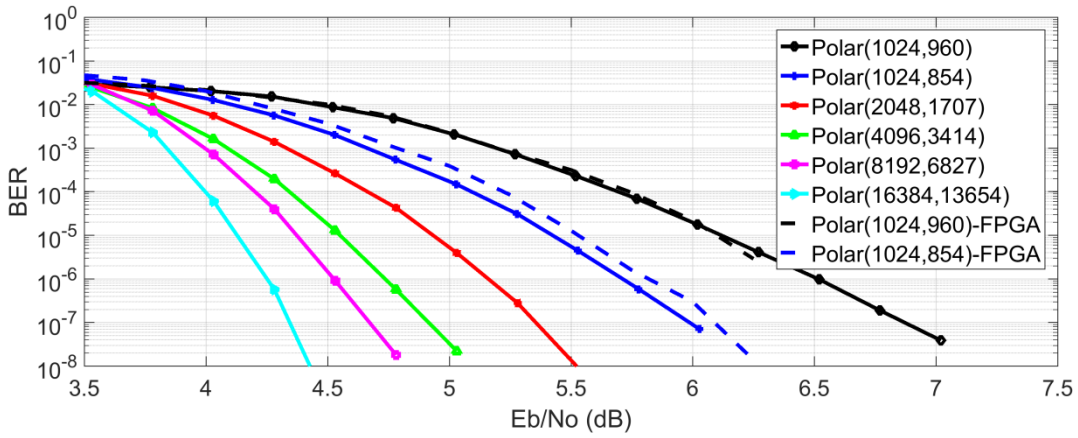

Figure 4: Simulation performance

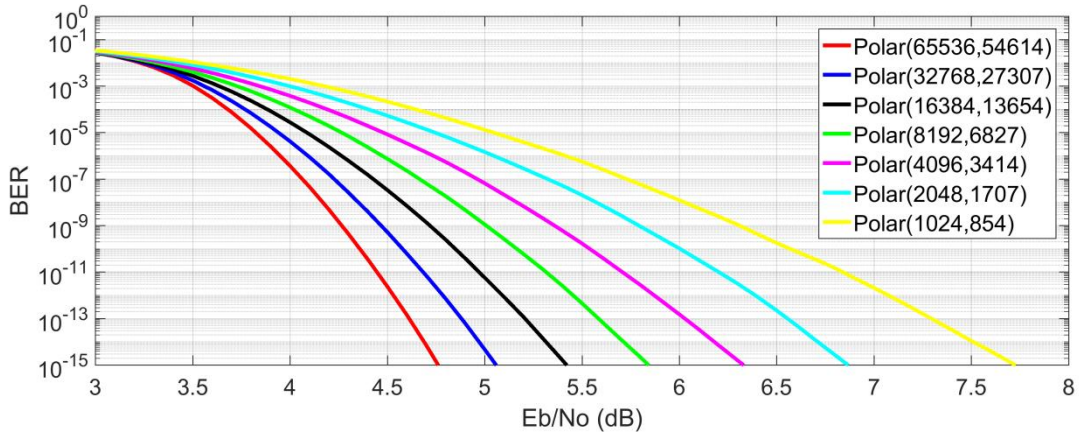

Figure 5: Theoretical performance

4. Conclusion

We proposed a polar encoder and a polar decoder that meet the requirements of the C-RAN fronthaul link. Both encoder and the decoder use systematic polar codes generated with BEC code design. The FPGA implementation results indicate that both encoder and decoder exceed 100 Gb/s throughput and the 10 dB coding gain is approached in N=8192 implementation. As a result, throughput, coding gain and coding overhead requirements of the C-RAN architecture are satisfied successfully.

References

1. E. Arikan, "Channel Polarization: A Method for Constructing Capacity-Achieving Codes for Symmetric Binary-Input Memoryless Channels," in *IEEE Transactions on Information Theory*, vol. 55, no. 7, pp. 3051-3073, July 2009.

2. G. Tzimpragos, C. Kachris, I. B. Djordjevic , M. Cvijetic, D. Soudris, and I. Tomkos, “A Survey on FEC Codes for 100G and Beyond Optical Networks,” IEEE Communications Surveys & Tutorials, vol. 18, no. 1, pp. 209–221, 2014.

3. A. Checko, H. L. Christiansen, Y. Yan, L. Scolari, G. Kardaras, M. S. Berger, and L. Dittman, “Cloud RAN for Mobile Networks - A Technology Overview,” IEEE Communications Surveys and Tutorials, vol. 17, no. 1, pp. 405–426, 2015.